Winston Chang Hall, Room 463
Department of Computer Science and Engineering
University of California Riverside, California, USA, 92521
mafar001@ucr.edu | afarinmahbod@gmail.com
Webpage : https://mahbod-afarin.github.io/
Github : https://github.com/mahbod-afarin
Phone : +1 (951)-512-3542

Mahbod Afarin

PhD Candidate, Computer Sciecne, University of California Riverside

Research Interests

- Computer Architecture
- Compiler Optimizations
- Hardware Accelerators
- GPU Architecture & Programming
- Graph Processing Algorithms & Accelerators
- Field Programmable Gate Arrays

Skills

- **Programming Languages**: C/C++, Python, CUDA, OpenMP, OpenCL, MATLAB.
- **Compiler**: LLVM, LLVM-BOLT, LLVM Machine Outliner, LLVM IR Outliner, and Propeller.
- **Hardware Design**: VHDL, Verilog HDL, SystemC, Xilinx ISE, Altera Quartus, Celoxica Agility Compiler, Synopsys Design Compiler.
- **Simulation Tools**: Multi2Sim, GPGPU-Sim, Mentor Graphics Modelsim, HSPICE, PSPICE, IC Encounter, HSIM, Cadence SoC Encounter, The Structural Simulation Toolkit.

Publications

- [***EuroSys'24***] X. Jiang, **M. Afarin**, Z. Zhao, N. Abu-Ghazaleh, R. Gupta, "Core Graph: Exploiting Edge Centrality to Speedup the Evaluation of Iterative Graph Queries," *2024 Proceedings of the Nineteen European Conference on Computer Systems (Acceptance Rate: **15.99%**)* (Contributed Equally with the First Author).
- [***MICRO'23***] C. Gao, **M. Afarin**, S. Rahman, N. Abu-Ghazaleh, R. Gupta, "MEGA Evolving Graph Accelerator," *2023 56th Annual IEEE/ACM International Symposium on Microarchitecture (Acceptance Rate: **22%**)* (Contributed Equally with the First Author).
- [***ASPLOS'23***] **M. Afarin**, C. Gao, S. Rahman, N. Abu-Ghazaleh, R. Gupta, "CommonGraph: Graph Analytics on Evolving Data," *International Conference on Architectural Support for Programming Languages and Operating Systems. (Acceptance Rate: **26.66%**)*
- [***HOPC'23***] **M. Afarin** et al., "CommonGraph: Graph Analytics on Evolving Data (Abstract)," *In Proceedings of the 2023 ACM Workshop on Highlights of Parallel Computing.*
- [***BigData'23***] A. Mazloumi, **M. Afarin**, R. Gupta, "Expressway: Prioritizing Edges for Distributed Evaluation of Graph Queries," *2023 IEEE International Conference on Big Data.*
- [***MICRO'21***] S. Rahman, **M. Afarin**, N. Abu-Ghazaleh, R. Gupta, "JetStream: Graph Analytics on Streaming Data with Event-Driven Hardware Accelerator," *2021 54th Annual IEEE/ACM International Symposium on Microarchitecture. (Acceptance Rate: **21.74%**)*
- [***Submitted***] **M. Afarin** et al., "UVVs: Identifying Unchanged Vertex Values in Evolving Graphs via Intersection-Union Analysis," *Proceedings of the 30th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming.*
- [***Submitted***] C. Gao, **M. Afarin**, X. Yin, N. Abu-Ghazaleh, R. Gupta, "Sagas: Temporally Consistent Sampling of Evolving Graphs," *2025 58th Annual IEEE/ACM International Symposium on Microarchitecture* (Contributed Equally with the First Author).

Awards & Achievements

- Won **UCR Dissertation Completion Fellowship Award** at UC Riverside, 2024.
- Received the **Excellent Service** badge in all three cycles of ASPLOS'24 Artifact Evaluation at ACM International Conference on Architectural Support for Programming Languages and Operating Systems, San Diego, 2024 (Certificate of Appreciation).
- Won **UCR GSA Travel Grant Award** at University of California, Riverside, 2023.
- Won **Dean's Distinguished Fellowship Award** at University of California, Riverside, 2019.
- **Ranked 7th** in terms of total GPA among 83 Computer Engineering students in Sharif University of Technology (**Top 8%**), 2018.
- Admitted as an **Exceptional Talent** at Sharif University of Technology for M.Sc, 2015.
- **1st Rank**, Achievement of the highest GPA in B.Sc among all Computer Engineering graduated students in Shahed University, 2015.

Research Experience

- **Research Intern**: Conducting research in the Inter-procedural Identical Basic Block Folding as part of the GCC compiler optimization team under the supervision of Dr. Sriraman Tallam at Google (*Sep' 24 - Jan' 25*).
- **Graduate Research Assistant**: Member of the GRaph Analytics with Scalibility & Performance (GRASP) research group (*Jan' 20 - Present*).
- **Graduate Research Assistant**: Member of the RIverside Programming Language & Software Engineering (RIPLE) research group (*Jan' 20 - Present*).
- **Graduate Research Assistant**: Member of Very Large Scale Integration Laboratory (VLSI-Lab) under supervision of Prof. Shaahin Hessabi (*Dec' 15 - Jan' 18*).

Education

- **Doctor of Philosophy** (Ph.D.), Computer Science, University of California Riverside, California, USA. *Jan' 20 - Present*
  - **Thesis**: *"Hardware-Software Approaches for Accelerating Graph Processing Workloads"*
  - **Advisors**: Professor Rajiv Gupta & Professor Nael Abu-Ghazaleh
  - **GPA**: **3.86**/4
- **Master of Science** (M.Sc.), Computer Engineering (Computer System Architecture), Sharif University of Technology, Tehran, Iran. *Sep' 15 - Jan' 18*
  - **Thesis**: *"Improving Manufacturing Yield and Life Cycle of Special Purpose SIMT Processors for Inexact Computing"* (**Thesis Grade**: Excellent)
  - **Advisors**: Professor Shaahin Hessabi
  - **GPA**: **4**/4 (**19.03**/20) (Ranked **7th** among 83 Computer Engineering students)
- **Bachelor of Science** (B.Sc.), Computer Engineering (Computer System Architecture), Shahed University, Tehran, Iran. *Sep' 11 - Jun' 15*
  - **Advisors**: Professor Naser Mohammadzadeh
  - **GPA**: **3.63**/4 (**17.53**/20) (Ranked **1st** among all Computer Engineering students)

Selected Research Projects

- **JetStream** (MICRO'21): **Event-Driven Hardware Accelerator for Streaming Graphs**
  UC Riverside, Riverside, CA *Jun 2020 – Apr 2021*
  - **First Streaming Graph Accelerator:** Developed JetStream, the first accelerator to support operations on streaming graphs (or dynamic graphs).
  - **New Asynchronous Streaming Algorithms:** JetStream subsumes the capabilities of GraphBolt and KickStarter software frameworks that allow edge deletions.
  - **Performance Improvements:** JetStream substantially outperforms software frameworks, especially with smaller batch sizes, making it well-suited for real-time analytics.
- **MEGA** (MICRO'23): **Evolving Graph Accelerator**
  UC Riverside, Riverside, CA *Jun 2022 – May 2023*
  - **First Evolving Graph Accelerator: MEGA** MEGA, the first accelerator for evolving graph workloads, provides support for multiple snapshots executing simultaneously.
  - **Batch-Oriented Execution:** Batch-oriented execution exploits the similarity of the graph across snapshots to reuse similar edge-fetches and minimize redundant execution of batches.
  - **Batch Pipelining:** We explore optimizations to the workflow to improve concurrency such as allowing multiple concurrent batches, and using pipelining across batches.
- **Common Graph** (ASPLOS'23): **Graph Analytics on Evolving Data**
  UC Riverside, Riverside, CA *Aug 2021 – Jun 2022*
  - **Converting Expensive Deletions to Additions:** Developed a method to convert deletions to additions in evolving graphs, improving work sharing and parallelism.

- **Triangular Grid Data Structure:** Designed the Triangular Grid structure to enhance work sharing across snapshots, employing a Steiner Tree formulation for optimal solutions.
- **New Graph Representation:** Designed a graph representation that avoids the need to mutate graphs and enables reuse of edges by snapshots that share them.

- **Core Graph** (EuroSys'24): **Exploiting Edge Centrality to Speedup the Evaluation of Iterative Graph Queries**
  UC Riverside, Riverside, CA *May 2021 – May 2023*
  - **Introduction of Core Graph (CG):** A novel proxy graph that is compact yet yields highly precise results, containing all vertices but only a subset of critical edges.
  - **Efficient CG Identification:** Algorithms to identify CG by solving a limited set of queries, efficiently pinpointing most non-zero centrality edges, ensuring the CG's effectiveness.
  - **Performance Improvement:** Significant performance gains in query evaluations across systems, notably cutting overhead and computation through the use of the CG structure.

- **Expressway** (BigData'23): **Prioritizing Edges for Distributed Evaluation of Graph Queries**
  UC Riverside, Riverside, CA *Jun 2023 – Aug 2023*
  - **Precise Results Using Highways:** Our study demonstrated that we can obtain precise results for most of the vertices by using only a small subset of the edges, i.e., *highways*.
  - **Algorithm for Identifying Highways:** We introduced a novel algorithm for identifying *highways* in a given graph.
  - **Distributed System:** Improved distributed graph query performance with a two-step algorithm: initially processing only the "highways," followed by a full graph evaluation.

Reviewing for Conferences & Journals

- **Conferences**: ASPLOS'26, BigData'25, CGO'25, MICRO'25, ISPASS'24, PPOPP'24, MICRO'23, ICDCS'23, ACM ICS'23, ISPASS'23, ICDCS'22, ISPASS'22, CGO'20, MICRO'20, PACT'20.
- **Journals**: CAL'23, TACO'23, IEEE Transaction on Computers'23, Parallel Computing'23.

Professional Services

- **Audio/Video Chair** of the ASPLOS'24 Conference.
- **Artifact Evaluation Committee:** ASPLOS'25, ASPLOS'24, ISCA'24.

Talks

- Present *Common Graph* and *Core Graph* projects at Society of Women Engineers, University of California, Riverside, Winter 2024.
- Present *Common Graph* project at Highlights of Parallel Computing Conference, Florida, USA, Spring 2023.

Teaching Experience

- Teaching Assistant, **Compiler Design** (Summer'21/22/23 and Spring'21/22), University of California, Riverside, Department of Computer Science & Engineering, Prof. Rajiv Gupta.
- Teaching Assistant, **System on Chip** (Spring'18) **Testability** (Fall'17) **Advanced VLSI** (Spring'17) **VLSI** (Fall'16), Sharif University of Technology, CE Dep., Prof. Shaahin Hessabi.
- Lab Instructor, **Logic Design Lab**, Sharif University of Technology, Department of Computer Engineering, Summer 2017, Prof. Siavash Bayat-Sarmadi.
- Lab Instructor, **Digital System Design Lab**, Sharif University of Technology, Department of Computer Engineering, Summer 2016, Prof. Maziar Goudarzi.
- Teaching Assistant, **VLSI Design** (Fall'19) **Computer Architecture** (Spring'19/Fall'19) **Digital Electronic** (Spring'19) **Logic Design Lab** (Spring'19) **Digital System Design Lab** (Spring'19), Shahed University, CE Department, Prof. Naser Mohammadzadeh.

Selected Course Projects

- Used **C++** to add a real kernel thread to *xv6* (*xv6* is an instructional OS consisting of a stripped-down version of *UNIX*) using a new system call, Advanced Operating System course project, Prof. Nael Abu-Ghazaleh, Spring 2021 ([Github]|[Overview]|[Report]).
- Used **C++** to implement the *lottery and stride scheduling*, and a system call that tracks the information about the system (information includes number of the process, system calls, and used pages) in *xv6*, Advanced Operating System course project, Prof. Nael Abu-Ghazaleh, Spring 2021 ([Github]|[Overview]|[Report]).
- Parallelize matrix multiplication using the *OpenMP* work-sharing *for* directive, as specified in the **OpenMP** API for **parallel programming**, Multiprocessor Architecture and Programming course project, Prof. Elaheh Sadredini, Winter 2022 ([Github]|[Overview]|[Report]).
- Improving the performance of **Sparse Matrix-Vector Multiplication** using *OpenMP*, Multiprocessor Architecture and Programming course project, Prof. Elaheh Sadredini, Winter 2022 (Github]|[Overview]|[Report]).
- Implementation of a **CUDA-based** histogram kernel showcasing the efficient use of *atomic operations* for parallel computation, GPU Architecture and Programming course project, Prof. Daniel Wong, Fall 2021 ([Github]|[Overview]|[Report]).
- Implementation of a ***tiled* matrix multiplication kernel** which can support arbitrary-sized matrices using *CUDA*, GPU Architecture and Programming course project, Prof. Daniel Wong, Fall 2021 ([Github]|[Overview]|[Report]).
- Implementing and optimizing the **reduction kernel** and analyzing basic architectural performance properties using *CUDA*, GPU Architecture and Programming course project, Prof. Daniel Wong, Fall 2021 ([Github]|[Overview]|[Report]).
- Improving the performance of Vector Addition program by finding the best *basic block* size using *CUDA*, GPU Architecture and Programming course project, Prof. Daniel Wong, Fall 2021 ([Github]|[Overview]|[Report]).
- Performance comparison of various GPU programming APIs (*OpenMP*, *CUDA*, *OpenCL*), GPU Architecture and Programming course project, Prof. Daniel Wong, Fall 2021.
- Implementation of the fundamental available expression analysis and **common sub-expression elimination** on LLVM using C++ language, Compiler Construction course project, Prof. Rajiv Gupta, Fall 2021 ([Github]|[Report]).
- Implementation of the fundamental **liveness analysis** as an *LLVM* pass using C++ language, Compiler Construction course project, Prof. Rajiv Gupta, Fall 2021 ([Github]|[Report]).
- Performance optimization of a matrix multiplication program via **register and cache reuse** using C++, High Performance Computing course project, Prof. Zizhong Chen, Fall 2021 ([Github]|[Overview]|[Report]).
- High performance sequential codes for **Solving Large Linear Systems**, High Performance Computing course project, Prof. Zizhong Chen, Fall 2021 ([Github]|[Overview]|[Report]).
- Parallel Sieve of Eratosthenes for Finding All Prime Numbers using **Open Message Passing Interface** (Open MPI), High Performance Computing course project, Prof. Zizhong Chen, Fall 2021 ([Github]|[Overview]|[Report]).
- Finding influencers in a network using Data Mining Techniques and SNAP Stanford Dataset collections, Data Mining course project, Prof. Vagelis Papalexakis, Spring 2021.
- Design and implementation of a O(m×n) space, O(m×n×k) time *SP Alignment Algorithm* for three DNA sequences using JAVA language, Algorithmic Techniques in Computational Biology course project, Prof. Tao Jiang , Spring 2021.
- Implementing the **Tomasulo Speculative Algorithm** using C++ language, Advanced Computer Architecture course project, Prof. Daniel Wong, Winter 2020 ([Github]|[Report]).
- Design and implementation of a **pipeline simulator** which supports **forwarding technique** using C++ language, Advanced Computer Architecture course project, Prof. Daniel Wong, Winter 2020 ([Github]|[Overview]|[Report]).

- Design and implementation of various **branch predictors**, including simple 1-bit and 2-bit predictors, as well as correlating (m,n) predictors using C++ language, Advanced Computer Architecture course project, Prof. Daniel Wong, Winter 2020 ([Github]|[Overview]|[Report]).
- Design and implementation of a cache, with support for **direct-mapped, set-associative, and fully-associative mapping**, Advanced Computer Architecture course project, Prof. Daniel Wong, Winter 2020 ([Github]|[Overview]|[Report]).
- Design and implementation of a **Search Engine** which allows users to search related tweets in the cryptocurrency area using Hadoop and Lucene, Information Retrieval and Web Search course project, Prof. Vagelis Hristidis, Winter 2020.
- Design, Simulation, and implementation of a complex ALU with exciting IP cores in ISE Design Suite (Xilinx), synthesized using Synopsis Design Compiler, System on Chip Design course project, Prof. Shaahin Hessabi, Fall 2017.
- **Post-layout simulation** for a complex ALU with **SoC Encounter**, System on Chip Design course project, Prof. Shaahin Hessabi, Fall 2017.
- Design, Simulation, and implementation of a serial divider at gate level and synthesize it with a scan chain, Testability course project, Prof. Shaahin Hessabi, Spring 2017.
- Implementing a software for simulating the impact of fault and delay on standard combinations logic with JAVA, Testability course project, Prof. Shaahin Hessabi, Spring 2017.
- Implementing a software for simulating ISCAS combinational circuits at gate level with JAVA, Testability course project, Prof. Shaahin Hessabi, Spring 2017.
- Investigation of Aging Mitigation Methods in Graphic Processing Units, Advanced Topics in Dependable Computing Systems project, Prof. Seyed-Ghassem Miremadi, Spring 2017.
- Investigation of the overhead of crosstalk avoidance codes for reliable data transfer of NoCs, Fault-Tolerant Systems Design, Prof. Seyed-Ghassem Miremadi, Fall 2016.
- Design and implementation of an arbiter circuit, along with determining its minimum die size using **SoC-Encounter**, Advanced VLSI Design, Prof. Shaahin Hessabi, Fall 2016.
- Finding the optimal W-min for an XOR_XNOR circuit to optimize power, PDP, and delay, Advanced VLSI Design, Prof. Shaahin Hessabi, Fall 2016.
- Designing, simulating, and implementing an arbiter circuit with **Verilog**, Modelsim, and Synopsis Design Compiler, and examining the effect of optimization constraints on speed and area, Advanced VLSI Design, Prof. Shaahin Hessabi, Fall 2016.
- Designing and simulating NAND gate in RTL logic and examining the effects of pull up resistor on the output load, Advanced VLSI Design, Prof. Shaahin Hessabi, Fall 2016.
- Design, Simulation, and Implementation of a Double Precision Floating Point Multiplier with **VHDL** and **ISE Design**, VHDL course project, Prof. Naser Mohammadzadeh, Spring 2014.
- Design, Simulation, and Implementation of **MIPS Processor** with **Verilog**, **ISE Design Suite, and Xilinx FPGA**, Computer Architecture laboratory course, Prof. Naser Mohammadzadeh, Spring 2014.
- Design and Implementation of Quoridor Game with Prolog, Artificial Intelligence course project, Prof. Shahrouz Moaven, Spring 2014.

References

- Professor Rajiv Gupta (My Ph.D. Supervisor – Email | Homepage)
- Professor Nael Abu-Ghazaleh (My Ph.D. Supervisor – Email | Homepage)
- Professor Shaahin Hessabi (My M.Sc. Supervisor – Email | Homepage)